Control Schemes for a Cascaded H-Bridge STATCOM

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Abstract: The conventional cascaded H - bridge converters suffers with demerits like more switching losses as it consists of series H- bridge cells. Moreover, the output voltage contains harmonics and often these, are beyond the acceptable limits. In the literature, various methods are available on zero sequence voltage and these techniques requires a large capacitor to inject voltage such capacitors are required whenever the unbalanced voltages appears in the system. The cause for unbalanced voltages is faults in the networks. It also suffers with practical issues with capacitor size. Similarly, the negative sequence voltage injection also suffers with handling issues and hence STATCOM is limited to certain range of capacitors only. This makes us to propose a new control technique to overcome such limitations. A combination of both zero sequence voltage and negative sequence currents are used to operate STATCOM. These techniques can handles the consequences due to unsymmetrical conditions arise from various system faults. This control technique is also used in cascaded H-bridge in STATCOM topology to improve the performance. MATLAB is used to test the effectiveness of the proposed method.

Keywords: H Bridge converter, STATCOM, system faults, zero sequence voltage, negative sequence current.

Introduction

H- Bridge inverter topology is widely used in converter models in semiconductor market. It has several advantages with less power losses and the harmonics generated across the output can also be observed in voltage waveform. Compared with all the multilevel converters H- Bridge multilevel converter needs less number of semiconductor devices and hence losses are less.

As due to low power losses, H- bride converters are useful for applications in power systems such as STATCOM. STATCOM handles only reactive power, will not handles active power. Each H- Bridge cell isolated with and capacitors, with number of capacitors a balancing problem in voltages arises in this topology [5], [7]. Generally power system experiences several fault conditions such as line to ground and line to line short circuit etc normally, high capacitor creates unbalance issues and in negative sequence current method, large capacitors are absent. This arrangement mitigates voltage unbalances [2].

Power systems faults creates disturbances in power system voltage, due to this unbalance current, flows in each phase of cluster. So, capacitor voltages will become unbalance. For proper operation of STATCOM, capacitor voltage balancing in each phase cluster is important. There are several methods of voltage balancing schemes like zero sequence voltage injection. This scheme requires a large margin for dc capacitor voltage compared with actual power system voltage during the fault conditions. Another method handles voltage unbalance of the capacitors independently by controlling of active power in each phase cluster. In this method power system voltage unbalance is not considered. The mentioned problems will create issue in proper functioning of STATCOM. To overcome issues another method if voltage balancing of capacitors is using negative sequence current. In this method large margin of capacitor voltage is not required for handling the power system voltage unbalance [12]. With this method, it is possible to eliminate the large margin of dc capacitor voltage under fault conditions and also output current of STATCOM can be controlled easily [11]. The validity is examined with digital simulation using MATLAB with different fault conditions such as line to ground and line to line short circuit conditions.

Capacitor Voltage Balancing Scheme

Determination of two opposite space vectors

The purpose of the capacitor voltage balancing scheme is to drive all capacitor voltages to a same value, which is the average of all nine capacitor voltages. Therefore, each capacitor voltage is defined as:

$$V_{cap}=V_{cap\ avg}+\hat{v}_{\text{cap}} \quad (1)$$

Where $V_{cap\ avg}$ is the average of all nine capacitor voltages and $\hat{v}_{cap}$ is the error of the capacitor voltage from the average value. By using two opposite space vectors two capacitors can be regulated during a switching period. Two capacitors having the maximum positive and maximum negative error voltages are selected to be discharged and charged, respectively. The remaining capacitor error voltages are unchanged and bounded by these two voltages [10].

It can be shown that for any given combination of the two capacitors a set of two opposite space vectors can be found that allows the desired capacitors charging and discharging. Our control implementation stores this data in a lookup table. Selection of two from the nine capacitors to be regulated during each switching period provides 36 possible combinations. In addition, there are four or five sets of opposite space vectors for each combination of two capacitors. The opposite space vectors are selected from a combination that provides largest current magnitude through the capacitor and hence the highest gain. If STATCOM is connected in the system, it should be operate effectively against various system faults.

This avoids the saturation of the control scheme by regulating a capacitor with a small (near zero) magnitude current. For example assume that the capacitors C_{Aa} and C_{Cc} have maximum negative and maximum positive error voltages respectively. Fig.1 shows switching device combinations that involve both capacitors. The switching device combinations in the left column involve capacitor C_{Aa} while those in the right column involve the capacitor C_{Cc} [9].

The terminal voltages generate from the switching device combinations in each row are opposite to each other hence so do the currents through capacitors C_{Aa} and C_{cc}. The switching device combination in the top left column generates the input side space vector (V_{cap}, $V_{cap}/\sqrt{3}$) and the output-side space vector ($0,-2V_{cap}/\sqrt{3}$) with the current ($I_a - I_c$) flowing through the capacitor C_{Aa}. When the input-side space vector is ($-V_{cap}$,$-V_{cap}/\sqrt{3}$) and the output side space vector is ($0, 2V_{cap}/\sqrt{3}$), then current ($-I_a$,I_c) flows through capacitor C_{Cc}.

Note that the opposite terminal voltages can also be generated by connecting the capacitors in the opposite direction. If the current ($I_A - I_c$) has a positive value, then the switching device combination on the top left column of Fig. 1 can be employed to charge the capacitor C_{Aa}, and the combination on the right column can be employed to discharge the capacitor C_{Cc}. However if the current ($I_a - I_c$) has a negative value then capacitors C_{Aa} and C_{Cc} can be charged and discharged by using the same combinations but connecting the capacitors in the opposite direction. Knowing the capacitor error voltage ($\hat{v}$) and current (I) determined from the space vectors the duty cycle d' of the opposite space vectors can be obtained from

$$d' = \frac{C}{T_s}\frac{|\hat{v}|}{|I|} \quad (2)$$

Where, T_s is the switching period of the converter. The maximum positive and the maximum negative error voltages in general have different magnitudes either can be employed in (1).

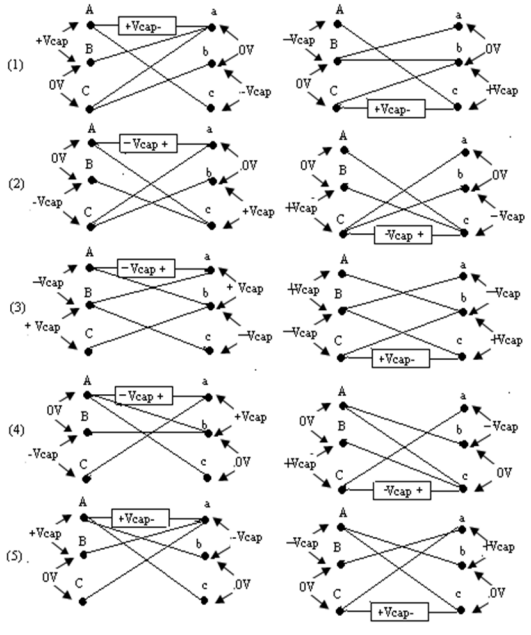

Figure 1. Switching device combinations involves different capacitors

Capacitor Voltage Stability

The ideal capacitor waveforms for the proposed capacitor voltage balancing scheme are illustrated in Fig. 2. During the first two subintervals the capacitors having the maximum positive and negative error voltages are driven toward the average capacitor voltage and then stay unchanged for the remaining subintervals [4].

The voltages of the remaining capacitors are unchanged throughout the switching period even though there are voltage ripples in the voltage of the capacitor employed in the remaining subintervals of the switching period. As described in the previous section the control scheme can charge and discharge any two capacitors during each switching period. In addition with the capacitor voltages defined as in (3), there are always capacitors with positive and negative error voltages.

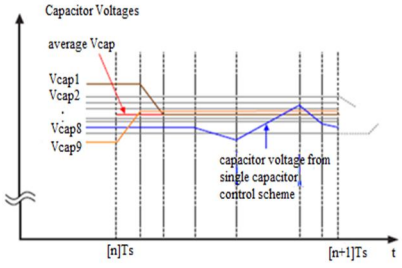

Figure 2. Space vector pattern in each switching period with the conventional and modified space vector modulation

The stability of the capacitor voltage can be proved by Lyapunov's approach. Lyapunov function is chosen to be

$$L = \sum_{j=1}^{9} \frac{1}{2} C \hat{v}_j^{\,2} \geq 0 \qquad (3)$$

Where, $\hat{v}_j$ is the error voltage of capacitor '*j*'. With the same capacitance for all nine switch cells, Eq. (4) can be expressed as,

$$L = \frac{1}{2} C \left[\hat{v}_n^{\,2} + \hat{v}_p^{\,2} + \cdots\cdots \right] \geq 0 \qquad (4)$$

Where $\hat{v}_p$ is the maximum positive error voltage and $\hat{v}_n$ is the maximum negative error voltage sampled at the beginning of the switching period. The other terms are the error voltages of the remaining capacitors. When the duty cycle *d'* is computed as in eqn. (2) using $\hat{v} = \hat{v}_p$, then the error voltage $\hat{v}_p$ is reduced to zero after one switching period and the corresponding charge is transferred to the capacitor associated with $\hat{v}_n$. The change in *L* is then equal to

$$\Delta L = \frac{1}{2} C \left[(\hat{v}_p + \hat{v}_n)^2 - \hat{v}_n^{\,2} \right] + \frac{1}{2} C \left[0 - \hat{v}_p^{\,2} \right] \qquad (5)$$

Since $\hat{v}_p$ is always positive and $\hat{v}_n$ is always negative ΔL of eqn. (5) is always negative. Hence, Lyapunov's stability theorem implies stability of this control algorithm. In practice a feedback loop for regulating the average capacitor voltage is necessary when the modular matrix converter is interfaced between a generator and an infinite-bus utility. Modeling and design of the control system for regulating the line currents and the average capacitor voltage is treated [3].

Static Synchronous Compensator (STATCOM)

The STATCOM is a solid-state-based power converter version of the SVC. Operating as a shunt-connected SVC its capacitive or inductive output currents can be controlled independently from its terminal AC bus voltage. Because of the fast-switching characteristic of power converters STATCOM provides much faster response as compared to the SVC. In addition in the event of a rapid change in system voltage the capacitor voltage does not change instantaneously therefore, STATCOM effectively reacts for the desired responses. For example, if the system voltage drops for any reason there is a tendency for STATCOM to inject capacitive power to support the dipped voltages [1-2]. STATCOM is capable of high dynamic performance and its compensation does not depend on the common coupling voltage. Therefore STATCOM is very effective during the power system disturbances.

Proposed Model and Basic Operation

The proposed circuit consists of three phase clusters shown in Fig.3. Each phase cluster consists of three H-bridge cells. The dc capacitor voltages are set to V_c,$2V_c$,$4V_c$ in a phase cluster. Fig. 4 shows describes the of output waveform. Voltage level from -7 to +7 can be generated by combining the capacitor voltages. The level is decided according to the calculation flow. Then the cluster outputs the nearest voltage level to reference V_a^*. Conventional cascaded H-bridge multilevel converter may require high number of H-bridge cells for low current distortion. But the proposed circuit configuration can output 15-level voltage in spite of only three cells. So conduction losses of semiconductor devices are as expected. For dc voltage balancing

in each phase cluster, the control method proposed here uses the fact that several switching patterns are available when a phase cluster outputs particular voltage levels. When a phase cluster outputs voltage Vc, there exists three operational pattern "V_c", "$2V_c$-V_c" and "$4V_c$-$2V_c$-V_c" charged or discharged capacitors are different.

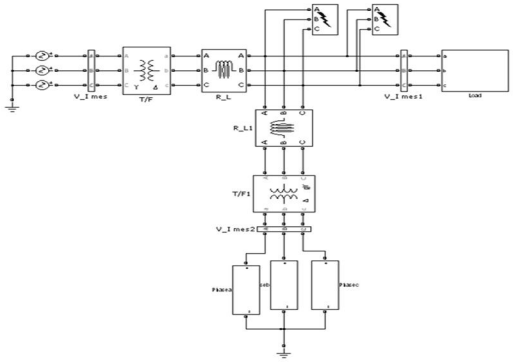

Figure 3. Main circuit configuration

These patterns are selected according to the relation between V_{c1}, V_{c2} and V_{c3}. When $4V_{c1} \geq 2V_{c2}$ and V_{c3} output pattern "V_c" is selected. When $2V_{c2} > 4V_{c1}$ andV_{c3} output pattern "$2V_c$-V_c" is selected. When $V_{c3} > 2V_{c2}$ and $4V_{c1}$ output pattern "$4V_c$-$2V_c$-V_c" is selected. To use same switching pattern in 1/4 cycle, the capacitor voltages are measured at 0, $\pi/2$, π, $3\pi/2$ (rad) of ac side phase angle.

All possible operational patterns and decision method is used when the polarities of STATCOM output voltage and current are same. "1" indicates that the cell outputs voltage to positive direction and its capacitor is discharged. "-1" indicates that the cell output voltage to negative direction and its capacitor is charged. It is similar when the polarity of the output current is opposite. By this method capacitor voltage ratio between H-bridge cells in a phase cluster is controlled.

Zero Sequence Voltage and Negative Sequence Current Control

The output waveforms are as shown in Fig.7, Fig.8, Fig. 9, Fig.10, Fig 11 and Fig.12. These are the STATCOM output voltage and current waveforms. In this waveforms the output current is balanced but the output voltage is exceeds the maximum value of voltage so this method does not requires the wide margin of dc capacitor voltage. In output waveforms0 t0 2 seconds power system voltage is under normal condition, from 2 to 4 seconds power system voltage experiences L-G fault condition and from 4 to 6 seconds power system voltage experiences L-L faults condition.

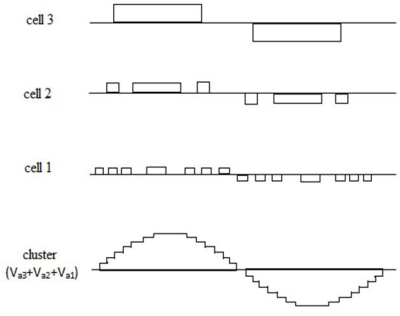

Figure 4. Example of output wave form

The proposed control method is based on the zero-sequence voltage and negative-sequence current, which is used exclusively depending on the extent of voltage unbalance. By this method, STATCOM can operate flexibly under normal power system condition and does not need wide margin of dc capacitor voltage under large asymmetrical condition. The validity is examined by digital simulation under one line and two-lines fault circuit condition. The simulation results showed the effectiveness of proposed STATCOM. In addition, proposed control scheme can be used for other type of applications such as photovoltaic inverter systems. It expands applicable scope of cascaded H-bridge multilevel converter.

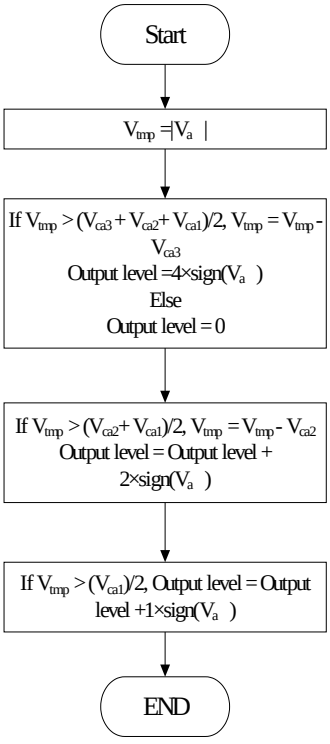

Figure 5. Decision method of output level

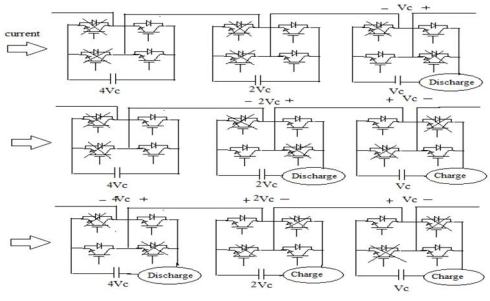

Figure 6. Capacitor voltage balancing between H-bridge cells

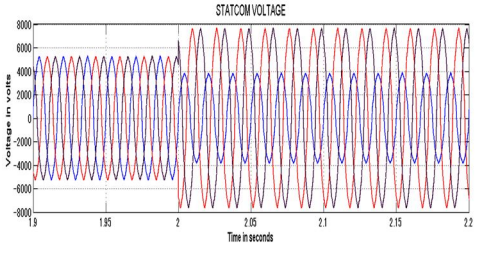

Figure 7. STATCOM voltage (L-G Fault)

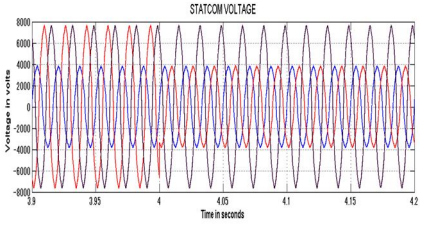

Figure 8. STATCOM voltage (LL Fault)

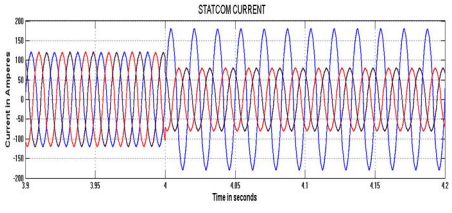

Figure 9. STATCOM current

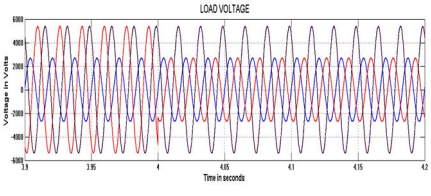

Figure 10. Capacitor voltages

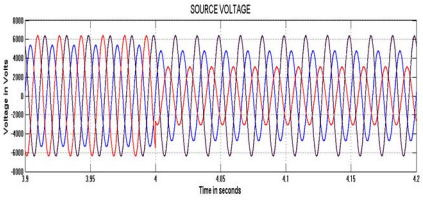

Figure 11. Source voltages

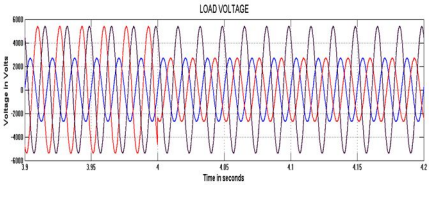

Figure 12. Load voltages

Conclusion

In this paper an effective configuration and control method is presented for a cascaded H-bridge STATCOM in three-phase power system. The proposed control method is based on the zero-sequence voltage and negative-sequence current, which is used exclusively depending on the extent of voltage unbalance. By this method, STATCOM can operate flexibly under normal power system condition and does not need wide margin of dc capacitor voltage under large asymmetrical condition. The validity is examined by digital simulation under one line and two-lines fault conditions. The simulation results show the effectiveness of proposed STATCOM. In addition, proposed control scheme can be used for other type of applications such as PV (photovoltaic) inverter systems. It expands applicable scope of cascaded H-bridge multilevel converter.

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